REMARKS

The Examiner rejected claim 1 under 35 U.S.C. § 102(e) as allegedly being anticipated by Wang *et al.* (U.S. Patent No. 6,924,560).

The Examiner rejected claims 1-8 under 35 U.S.C. § 102(e) as allegedly being anticipated by Chang (U.S. Patent Application Publication No. 2005/0224878).

Applicants respectfully traverse the § 102 rejections with the following arguments.

35 U.S.C. § 102(e)

The Examiner rejected claim(s) 1 under 35 U.S.C. § 102(e) as allegedly being anticipated by U.S. Patent No. 6,924,560 to Wang *et al.*

Applicants respectfully contend that Wang does not anticipate claim 1, because Wang does not teach each and every feature of claim 1. For example, Wang does not teach "a back gate region **abutting** and **being sandwiched** between the first and second FinFET active regions" of claim 1 (bold emphasis added).

Firstly, the Examiner argues in bullet #7 of the Office Action that in FIG. 2 of Wang, the back gate region 226 abuts the first and second FinFET active regions 202, 206. In response, Applicants note that even if the metal 226 was considered a back gate region 226, the back gate region 226 would **not abut** the first and second FinFET active regions 202, 206. In fact, the back gate region 226 is at a different level ("second level" – column 4, lines 1-3 of Wang) than the first and second FinFET active regions 202, 206; therefore the back gate region 226 could not abut the first and second FinFET active regions 202, 206. In contrast, according to claim 1, the back gate region **abuts** the first and second FinFET active regions.

Secondly, the Examiner argues in bullet #7 of the Office Action that in FIG. 2 of Wang, the back gate region 226 is sandwiched between the first and second FinFET active regions 202, 206. In response, Applicants note that even if the metal 226 was considered a back gate region 226, the back gate region 226 would **not be sandwiched between** the first and second FinFET active regions 202, 206. In fact, the back gate region 226 is at a different level ("second level" – column 4, lines 1-3 of Wang) than the first and second FinFET active regions 202, 206; therefore the back gate region 226 could not be sandwiched between the first and second FinFET active

regions 202, 206. In contrast, according to claim 1, the back gate region is **sandwiched between** the first and second FinFET active regions.

Based on the preceding arguments, Applicants respectfully maintain that Wang does not anticipate claim 1, and that claim 1 is in condition for allowance.

The Examiner rejected claims 1-8 under 35 U.S.C. § 102(e) as allegedly being anticipated by U.S. Patent Application Publication No. 2005/0224878 by Chang.

Applicants respectfully contend that Chang does not anticipate claim 1, because Chang does not teach each and every feature of claim 1. For example, Chang does not teach "the first FinFET active region includes at least first and second devices... wherein the back gate region is **shared by the first and second devices**" of claim 1 (bold emphasis added).

Firstly, Applicant note that FIG. 14 of Chang is not a structure illustration but only a circuit diagram showing the electrical interconnection between different regions of the structure in FIG. 13 of Chang. Therefore, FIG. 14 of Chang does not teach any features of claim 1.

Secondly, the Examiner argues in bullet #8 of the Office Action that in the art of Chang the back gate region is shared by the first and second devices. In response, Applicants note that in FIG. 13 of Chang, the back gate region is **not shared by the first and second devices**. It should be noted that according to claim 1, the first FinFET active region includes at least first and second devices. According to FIG. 13 of Chang, the first FinFET active region is one of the bars which are parallel to the line 92 and have source regions 62, 63 and drain region 90. It can be seen in FIG. 13 of Chang that each of the first and second devices of the first FinFET active region has a **separate** back gate region. For example, on the first FinFET active region, the first device which has a front gate 75 and a source region 62, has a separate back gate region 65; the

second device (the next one) has another separate back gate region 66 (FIG. 13 of Chang). In contrast, in claim 1, **the first and second devices share** the same back gate region.

Based on the preceding arguments, Applicants respectfully maintain that Chang does not anticipate claim 1, and that claim 1 is in condition for allowance.

The Examiner rejected claim 2 under 35 U.S.C. § 102(e) as allegedly being anticipated by U.S. Patent Application Publication No. 2005/0224878 by Chang. Since claim 2 depends from claim 1 which is not anticipated by Chang as argued above, Applicants contend that claim 2 is likewise in condition for allowance.

Moreover, applicants respectfully contend that Chang does not anticipate claim 2, because Chang does not teach each and every feature of claim 2. For example, Chang does not teach "the second FinFET active region includes at least third and fourth devices, and wherein the back gate region is **shared by the third and fourth devices**" of claim 2 (bold emphasis added).

Firstly, Applicant note that FIG. 14 of Chang is not a structure illustration but only a circuit diagram showing the electrical interconnection between different regions of the structure in FIG. 13 of Chang. Therefore, FIG. 14 of Chang does not teach any features of claim 2.

Secondly, the Examiner argues in bullet #8 of the Office Action that in the art of Chang the back gate region is shared by the third and fourth devices. In response, Applicants note that in FIG. 13 of Chang, the back gate region is **not shared by the third and fourth devices**. It should be noted that according to claim 2, the second FinFET active region includes at least third and fourth devices. According to FIG. 13 of Chang, the second FinFET active region is one of the bars which are parallel to the line 92 and have source regions 62, 63 and drain region 90. It

can be seen in FIG. 13 of Chang that each of the third and fourth devices of the second FinFET active region has a **separate back gate region**. For example, on the second FinFET active region, the third device which has a front gate 75 and a source region 62, has a separate back gate region 65; the fourth device (the next one) has another separate back gate region 66 (FIG. 13 of Chang). In contrast, in claim 2, **the third and fourth devices share** the same back gate region.

Based on the preceding arguments, Applicants respectfully maintain that Chang does not anticipate claim 2, and that claim 2 is in condition for allowance.

The Examiner rejected claims 3-5 under 35 U.S.C. § 102(e) as allegedly being anticipated by U.S. Patent Application Publication No. 2005/0224878 by Chang. Since claims 3-5 depend from claim 1 which is not anticipated by Chang as argued above, Applicants contend that claims 3-5 are likewise in condition for allowance.

The Examiner rejected claim 6 under 35 U.S.C. § 102(e) as allegedly being anticipated by U.S. Patent Application Publication No. 2005/0224878 by Chang. Since claim 6 depends from claim 1 which is not anticipated by Chang as argued above, Applicants contend that claim 6 is likewise in condition for allowance.

Moreover, applicants respectfully contend that Chang does not anticipate claim 6, because Chang does not teach each and every feature of claim 6. For example, Chang does not teach "the N substructures comprise M **SRAM memory cells**" of claim 6 (bold emphasis added).

The Examiner argues in bullet #8 of the Office Action that Chang discloses the semiconductor structure wherein the N substructures comprise M SRAM memory cells. In response, Applicant note that Chang does not disclose the N substructures comprise M SRAM memory cells. In fact, Chang **does not teach SRAM memory cells**. More specifically, in the

entire Chang's Patent including FIG. 13, different regions are interconnected to form DRAM cells (line 1 of Abstract; para [0002], line 1; para [0033], line 4; para [0052], line 1). In contrast, claim 1 **claims SRAM memory cells**.

Based on the preceding arguments, Applicants respectfully maintain that Chang does not anticipate claim 6, and that claim 6 is in condition for allowance.

The Examiner rejected claim 7-8 under 35 U.S.C. § 102(e) as allegedly being anticipated by U.S. Patent Application Publication No. 2005/0224878 by Chang. Since claim 7-8 depend from claim 1 which is not anticipated by Chang as argued above, Applicants contend that claim 7-8 are likewise in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

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